Sahasrajit Sarmasarkar

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Research interests

Learning Theory, Distributed Coded Computation and Information Theory

Education

Indian Institute of Technology Bombay

B.Tech and M.Tech in Electrical Engineering *July '16 - July '21*

Specialisation: Communication and Signal Processing

- Major GPA – **9.74/10.0** (**Second** in a batch of nearly 72 students)
- Minor degree in *Computer Science & Engineering*

Publications

- **S. Sarmasarkar**, K.S. Reddy and N. Karamchandani "Query Complexity of Heavy-Hitter distribution", presented in International Symposium On Information Theory, 2021 (https://arxiv.org/abs/2005.14425)
- **S. Sarmasarkar**, V. Lalitha and N. Karamchandani "On Gradient Coding with Partial Recovery", presented in International Symposium On Information Theory, 2021 (https://arxiv.org/abs/2102.10163)

Research Projects

Query Complexity of Heavy-Hitter distribution *Aug '19 - Ongoing*

Guide: Prof. Nikhil Karamchandani *Electrical Engineering, IIT Bombay*

Introduction: We study the problem of identifying the subset of elements in the support of an underlying discrete distribution $\mathcal{P}$ whose probability is larger than some threshold γ, by actively querying an oracle to gain information about a sequence $X_1, X_2, \ldots$ of $i.i.d.$ samples drawn from $\mathcal{P}$ under two different query models (a) each query is an index i and the oracle return the value X_i and (b) each query is a pair (i, j) and the oracle gives a binary answer confirming if $X_i = X_j$ or not.

- We propose upper bounds on the query complexity of our algorithm and also derive "matching" lower bounds on any optimal algorithm under both the query models.
- We also consider noisy versions of the two query models and propose upper bounds on algorithms to estimate the desired subset of elements.
- We prove "matching" upper and lower bounds for an alternate problem where the aim is to identify any subset of r support elements with probability above γ under the first query model.

Multi-tasking policies in distributed computation | [Report] *Jan '20 - Ongoing*

Guide: Prof. Harish Pillai *Electrical Engineering, IIT Bombay*

Introduction: We study the problem of redundancies during distributed computation. We are given a set of n jobs(tasks) and c servers and the goal is to distribute k distinct jobs to each server such that each job appears in exactly r distinct servers. We attempt to create distributions to ensure minimum redundancies in jobs when a set of x servers chosen uniformly at random return their jobs.

- We prove that the expectation of the number of distinct jobs is same irrespective of the distribution chosen.
- We design a sufficient criterion such that the variance of the number of distinct jobs for any x would be the least amongst all distributions.
- We find that constructions using Balanced Incomplete Block Designs satisfies the sufficiency condition for certain values of n and k.

Straggler mitigation under gradient coding *Aug '20 - Ongoing*

Guide: Prof. Nikhil Karamchandani, Prof. Lalitha Vadlamani *Electrical Engineering, IIT Bombay*

Introduction: This is a synchronous gradient coding problem where the master does not expect the sum of all the k-gradients but the sum of any $l = \alpha.k$ gradients would suffice. Each of the n child servers is provided with a set of gradients to compute and transmit one or more linear combinations of them. We aim to design schemes which could tolerate upto s-stragglers with minimum number of gradients per worker.

- Designed schemes attaining the lower bound on the number of gradient data subsets assigned to every worker but with high communication load per worker.
- We also simulate such schemes using different delay model on machines and show empirically that such schemes may indeed converge faster than full recovery schemes and the ones which don't use any coding.

Work Experience

Carry Save Adder Network Optimisations *May '19- July '19*

Texas Instruments

- Devised algorithms for connections of input and output pins of full adder cells so as to minimise the maximum delay of the whole carry-save adder network.
- Worked on buffer insertion problem and used linear programming to insert buffers so that the whole network could be wave-pipelined.
- Worked on cell-selection problem to meet a certain delay target of the whole network with the lowest cost.
- Implemented all the above algorithms using actual delay data of cells as per 65nm node technology to incorporate slew and loading of cells and generalised the algorithms to any combinational network.

IIT Bombay Racing (Electric Subsystem) *Academic year 2017-19*

A cross functional team of **60+** students from **7** engineering disciplines which designs and fabricates an **electric race car** for **Formula Student** competition held annually at **Silverstone, UK**.

Design Engineer *Jul '18- May '19*

- Designed the harness of the whole car keeping into considerations the current and voltage rating of each input signal in each board.
- Designed and tested the **CAN (Controlled Area Network)** node using CAN enabled micro-controller atmega-16M1 in embedded C using interrupts for sending and receiving messages.

Junior Design Engineer *Aug '17- Jun '18*

- Developed codes using interrupts in **ECU (embedded C programming)** for reading data from **CAN bus**, processing and sending control commands to **BLDC (Brushless DC motors)** on CAN bus.

Stereo-Camera Calibration & Image Rectification on FPGA *Summer 2018*

Guide: Prof. Sachin Patkar *Electrical Engineering, IIT Bombay*

- Developed a dual **OV7670 camera** setup compatible with **De0-Nano Board (Cyclone IV-E FPGA)**.
- Used FTDI chip **FT245RL** for sending bytes captured by camera in default **YUV** format through **serial port** communication with PC by writing VHDL and Verilog codes.
- Used **OpenCV library** on C++ for image construction from the received bytes on the serial port of PC.

Scholastic Achievements & Awards

- Scored a Semester Performance Index **10/10** in the seventh and eighth semesters at IIT-Bombay
- Awarded the **Institute Academic Prize** for standing first (out of 72) in 2020.
- Awarded **AP** grades (given to top 1 % of the class) in 3 courses: MA 105 (Calculus), PH 107 (Quantum Physics and Applications) and EE 225 (Network Theory).
- Achieved **All India Rank 1** in **Kishore Vaigyanik Protsahan Yojana (KVPY) 2016** conducted by **Indian Institute of Science,Bangalore** out of nearly **100,000** candidates.
- Secured **All India Rank 98 and 49** in **Joint Entrance Examination (Advanced) 2016** and **Joint Entrance Examination (Mains) 2016** respectively among 1.4 million students.
- Attended the **OCSC (Orientation-Cum Selection Camp)** for being amongst the top-35 students in **Indian National Physics Olympiad** conducted by **HBCSE Mumbai**.
- Accepted into **B.Stat** program in **ISI (Indian Statistical Institute) Calcutta** (offered to top **60** students) amongst nearly **40,000** applicants.
- Awarded the prestigious **National Talent Search Examination (NTSE)** scholarship in 2014 by the **HRD ministry** of Government of India, awarded to **1000** students across the country.

Select Key Projects

Iterative decoding algorithms on modern codes | [Slides] *Jan '20 - May '20*

Guide: Prof. Manoj Gopalkrishnan, Prof. Nikhil Karamchandani *Electrical Engineering, IIT Bombay*

The goal in this project was to do an existing literature survey on modern LPDC (Low Density Parity Check) codes and turbo codes.

- Studied the classical message passing algorithm on linear codes and the convergence in error probability of belief propagation algorithm on certain ensembles of LDPC codes under certain symmetric channels.
- Understood EXIT charts to get an information theoretic viewpoint of the decoding process and read about the convergence of the peeling decoder of LDPC codes under Binary erasure channel.
- Studied turbo codes, their representations as factor graphs, the density evolution process during iterative decoding, stability condition, their corresponding EXIT charts and their weight distribution.

CoVID-19 Pandemic Spread Analysis | **[Report]** *Mar '20 - Apr '20*
Guide: Prof. D. Manjunath *Electrical Engineering, IIT Bombay*
We attempted to model the early spreading of CoVID-19 in India and other countries using variations of graphical SIR(Susceptible Infected Recovered) models.
- Studied various SIR models to approximately model the spread rate of CoVID-19 in India.
- Three different models were simulated for four different countries to estimate the contact rates using the data available on the number of cases.

Hardware Accelerator for Graphics Computation | **[Report]** *Oct '19 - Nov '19*
Guide: Prof. Madhav Desai *Electrical Engineering, IIT Bombay*
The goal in this project was to build an efficient hardware accelerator which exploits parallelism.
- Implemented a pipelined design for convolving a kernel with an image stored in a shared memory.
- Parallelized the operation using multiple engines which can fetch the image through pipes and perform convolution to reduce computation time and utilize the entire memory bandwidth.

Superscaler and Pipelined Processor Design *Oct '18 - May '19*
Guide: Prof. Virendra Singh *Electrical Engineering, IIT Bombay*
Implemented general purpose micro-processor designs with an instruction set architecture having 16 diverse instructions in VHDL.
- **Pipelined RISC processor implementation** *Oct '18 - Nov '18*
  Employed hazard-mitigation, operand-forwarding techniques to design a six stage execution pipeline and synthesized on Altera Deo-Nano FPGA Board running at 50 MHz.
- **Superscaler processor implementation** *Apr '19 - May '19*
  Designed an out of order execution engine consisting of two way fetch supported by specialised execution engines, reorder buffer, register renaming and reservation station to extract instruction level parallelism.

Teaching Responsibilities

Institute Teaching Assistant

Served as a Teaching Assistant for **MA 106 (Linear Algebra)** (Spring '18), **MA 105 (Calculus)** (Autumn '18), **MA207 (Differential Equations-II)** (Summer '18) and **EE 325 (Probability and Random Processes)** (Autumn '20)
Conducted weekly tutorial sessions for a group of 40 students, involved in problem solving and concept discussion sessions, engaged in design and grading of exams.

Relevant Courses

Electrical Engineering	Random Graphs, Information Theory and Coding, Error Correcting Codes, Digital Communications, Number Theory and Cryptography
Computer Science	Machine Learning, Data Structures & Algorithms, Computer Networks, Design and Analysis of Algorithms
Mathematics and Statistics	Advanced Concentration Inequalities, Markov Chains & Queueing Systems, Probability & Random Processes, Games & Information*

* In Progress

Technical Skills

Programming Skills: C/C++, Python, Verilog, VHDL, LaTeX
Softwares & Tools: Scilab, MATLAB, Octave, Eagle, NGSPICE, Gnuplot, Wireshark, Quartus Prime

Extra Curricular Activities

- Completed a **yearlong** training in National Cadet Corps(NCC) and participated in **Republic Day Camp**.
- Presented my internship experience at Texas Instruments at **BLAH** organised by **Electronics and Robotics Club, IIT-B**.
- Earned **third** position in **Logic GC**-2018 by Maths and Physics Club.
- Secured **3rd** position in **Electric Jhatka** GC-2017 by the Electronics Club.